

Amendments to the Claims:

Claims 1, 4 and 6 have been amended. No new matter is introduced in these amendments.

5 Claims 2-3, 16, 20, and 24 are cancelled without disclaimer to the subject matter thereof.

No new claims or new matter have been added.

Listing of Claims:

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This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A keyboard comprising:

15 a key module comprising a plurality of at least one key cell cells with each having an output end being selectively connected to one of a first voltage while being pressed and a second voltage while not being pressed;

a detect circuit electrically connected to the outputs end of the key cell cells for generating a control signal whenever one of the output end of the key cell becomes connected to the other of the second voltage and the first voltage, wherein the detect circuit comprises an amplifying circuit and a plurality of capacitors each having a first end being coupled to the output end of each of the key cells, respectively, and having a second end;

25 a parallel-to-serial register electrically connected to the output end of the key module; and

30 a processor electrically connected to the parallel-to-serial register and the detect circuit for controlling the parallel-to-serial register according to the control signal without polling for a status of the key cells during a time period between any key cell being connected to the

first voltage and then connected to the second voltage;
wherein the second ends of the capacitors are connected together and
coupled to the amplifying circuit, and the amplifying circuit is
configured for amplifying a voltage in one of the capacitors and has
5 an output end for outputting the amplified voltage; and
wherein the control signal is generated according to the amplified
voltage.

2. (cancelled)

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3. (cancelled)

4. (currently amended) The keyboard of claim 31, wherein the detect circuit further comprises a set of comparators electrically connected to the amplifying circuit, for comparing whether the amplified voltage ~~output from~~
15 ~~an output end of the amplifying circuit~~ is in a predetermined range and generating the control signal accordingly.

5. (previously presented) The keyboard of claim 4, wherein the set of
20 comparators comprises a positive comparator for generating the control signal when the voltage output from the output end of the amplifying circuit exceeds a positive reference voltage, and a negative comparator for generating the control signal when the voltage output from the output end of the amplifying circuit is lower than a negative reference voltage.

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6. (currently amended) The keyboard of claim 45, wherein the detect circuit further comprises an OR gate with its input ends electrically connected to the output ends of the set of comparators, and its output end for outputting the control signal.

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7. (previously presented) A keyboard comprising:

- a key module comprising at least one key cell with an output end;
- a detect circuit electrically connected to the output end of the key cell for detecting a transient voltage at the moment when the key cell is pressed and released and generating a corresponding control signal;
- 5 a parallel-to-serial register electrically connected to the output end of the key module; and
- a processor electrically connected to the parallel-to-serial register and the detect circuit for controlling the parallel-to-serial register only upon reception of the control signal without polling for a status of the key cells during a time period between any key cell being pressed and then released.
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- 8. (previously presented) The keyboard of claim 7, wherein the detect circuit comprises at least one capacitor corresponding to and electrically connected to the at least one key cell within the key module for detecting the transient voltage.
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- 9. (previously presented) (previously presented) The keyboard of claim 8, wherein the detect circuit further comprises a comparator electrically connected to the capacitor for generating the control signal by comparing the transient voltage with a reference voltage.
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- 10. (previously presented) The keyboard of claim 9, wherein the detect circuit further comprises an amplifier electrically connecting the capacitor and the comparator for amplifying the transient voltage.
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- 11. (previously presented) The keyboard of claim 8, wherein the detect circuit further comprises a set of comparators electrically connected to the capacitor for generating the control signal by comparing the transient voltage with reference voltages.
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12. (previously presented) The keyboard of claim 11, wherein the set of comparators comprises a positive comparator and a negative comparator for comparing the transient voltage with a positive reference voltage and a negative reference voltage, respectively, to generate the control signal.

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13. (previously presented) The keyboard of claim 12, wherein the detect circuit further comprises an amplifier electrically connecting the capacitor and the set of comparators for amplifying the transient voltage.

10 14. (previously presented) The keyboard of claim 12, wherein the detect circuit further comprises an OR gate electrically connected to the set of comparator for outputting the control signal.

15. (previously presented) The keyboard of claim 14, wherein the detect circuit further comprises an amplifier electrically connecting the capacitor and the set of comparators for amplifying the transient voltage.

16. (cancelled)

20 17. (previously presented) A keyboard comprising:
a key module comprising at least one key cell with an output end;
a detect circuit electrically connected to the output end of the key cell for
detecting a transient voltage at the moment when the key cell is
pressed and released and generating a control signal;
25 a parallel-to-serial register electrically connected to the output end of the
key module for inputting input data from the output end when the
key cell is pressed and released; and
a processor electrically connected to the parallel-to-serial register and the
detect circuit for controlling the parallel-to-serial register and
30 reading the input data therein only upon reception of the control
signal without polling for a status of the key cells during a time

period between any key cell being pressed and then released.

18. (previously presented) The keyboard of claim 1, wherein the key module further includes a plurality of key cells each having an output end connected to one of the first voltage and the second voltage; and the parallel-to-serial register is electrically connected to the output end of each of the key cells in the key module for reading a parallel input being the voltages at the output end of all the key cells and converting the parallel input into a serial representation for output to the processor.

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19. (previously presented) The keyboard of claim 7, wherein the key module further includes a plurality of key cells each having an output end; and the parallel-to-serial register is electrically connected to the output end of each of the key cells in the key module for reading a parallel input being voltages at the output end of all the key cells and converting the parallel input into a serial representation for output to the processor.

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20. (cancelled)

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21. (previously presented) The keyboard of claim 17, wherein the key module further includes a plurality of key cells each having an output end; and the parallel-to-serial register is electrically connected to the output end of each of the key cells in the key module for inputting parallel input data being voltages at the output end of all the key cells and converting the parallel input data into a serial representation for output to the processor.

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22. (previously presented) The keyboard of claim 1, wherein the detect circuit is further for asserting the control signal only while detecting a transient voltage being greater than a reference voltage, the transient voltage corresponding to a change in voltage at the output end of the key cell and being a voltage spike that occurs at the moment the output end of the key cell becomes connected to the

other of the second and the first voltage.

23. (previously presented) The keyboard of claim 7, wherein the detect circuit is further for asserting the control signal only while detecting the transient voltage being greater than a reference voltage, the transient voltage being a voltage spike that occurs at the moment the key cell is pressed and at the moment the key cell is released.

10 24. (cancelled)

25. (previously presented) The keyboard of claim 17, wherein the detect circuit is further for asserting the control signal only while detecting the transient voltage being greater than a reference voltage, the transient voltage being a voltage spike that occurs at the moment the key cell is pressed and at the moment the key cell is released.

15 26. (previously presented) A keyboard comprising:

20 a plurality of key cells each having an output end connecting to either a first voltage or a second voltage;

a plurality of capacitors including one capacitor with a first end being coupled to the output end of each of the key cells;

25 an amplifier being coupled to a second end of each of the capacitors;

a first comparator having a positive input terminal coupled to an output end of the amplifier and having a negative input terminal coupled to a positive reference voltage;

30 a second comparator having a negative input terminal coupled to the output end of the amplifier and having a positive input terminal coupled to a negative reference voltage;

a logical OR gate having input ends coupled to output ends of the first and second comparators and having an output end being a control signal for being coupled to a processor to indicate that one of the key cells

has been pressed and to indicate that one of the key cells has been released; and

5 a parallel-to-serial register having parallel input lines coupled to the output end of each of the key cells and having a serial output line for being coupled to the processor, without the processor polling for a status of the key cells during a time period between any key cell being pressed and then released.